Automated Analog Model Generation for High Quality Verification using Event Driven Simulators

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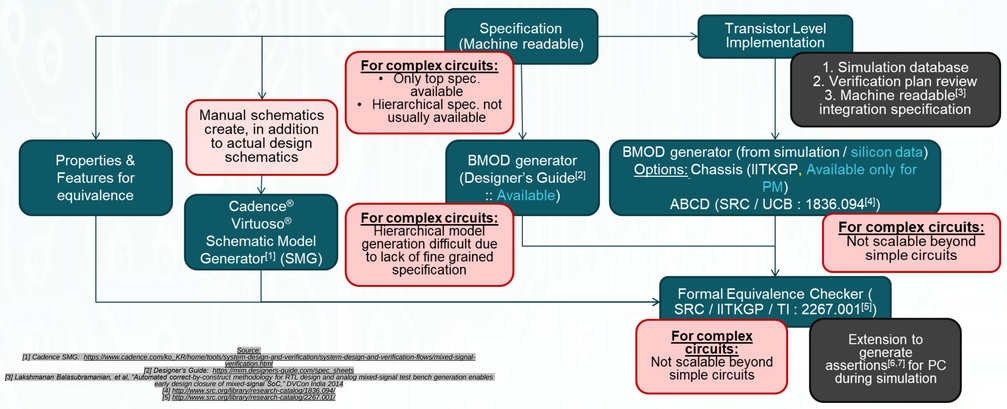
1. Motivation & Problem Statement (1/2)

Introduction

- Verification of a complex System on Chip (SoC)
  - Involves considerable manual effort in creating models for analog circuits
  - Conventional model generation methods have limitations
  - Non-scalable, involve significant manual effort, not true to implementation
  - Scalar real numbered (RN) models can only represent either voltage or current quantity
- Machine Learning (ML) based model learning from IP simulations[8]
  - Comprehensiveness and fidelity limited to the set of stimuli and simulation conditions encountered during learning
  - Any new scenario is an outlier for the ML based model

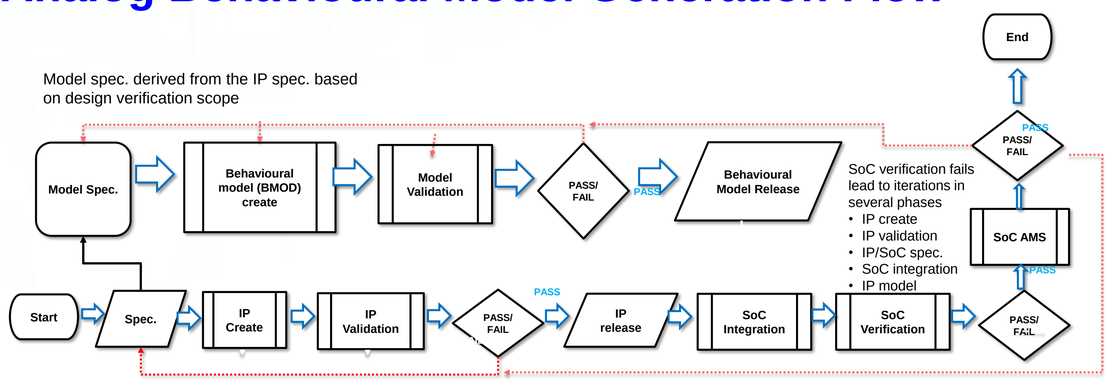
Motivation and Problem Statement

- Analog mixed-signal (AMS) co-sim. scope reduction to improve SoC execution cycle time
  - Typical low power (LP), mixed-signal (MS), embedded processing (EP) SoCs
  - AMS co-sim. cycle time: 1 to 3 weeks of runtime covering RTL stage and GL stage across multiple corners and hundreds of testcases
- Digital mixed-signal (DMS) co-sim.
  - Much efficient
  - Depend on manually created models, questionable quality and comprehensiveness
- Fault coverage – Crucial parameter to measure quality of integrated circuit test
  - Quite mature and fully automated for digital circuits
    - Automatic test pattern generation (ATPG), leakage current, and scan methods
  - For Analog ICs, tools to analyse test cost and quality lag behind
  - The fault grading directly impacts product cycle time, time to market, and overall cost
  - Current analog defect simulation flow too slow and inefficient to be of practical value[9]
- Increasingly complex integration of various components on mixed-signal systems
  - Higher quality for automotive functional safety and safety-critical systems
  - Standards (IEEE P2427 & ISO 26262) focusing more on analog defect coverage



Source:
[1] Cadence SMG: https://www.cadence.com/ko_KR/home/tools/system-design-and-verification/system-design-and-verification-flows/mixed-signal-verification.html
[2] Designer's Guide: https://mtm.designers-guide.com/spec_sheets
[3] Lakshmanan Balasubramanian, et al, "Automated correct-by-construct methodology for RTL design and analog mixed-signal test bench generation enables early design closure of mixed-signal SoC," DVCon India 2014
[4] http://www.src.org/library/research-catalog/1836.094/
[5] http://www.src.org/library/research-catalog/2267.001/
[6] Pooja Sundar, et al, "Assertion based self-checking of analog circuits for circuit verification and model validation in SPICE and co-simulation environments," DVCon 2011
[7] Pooja Sundar, et al, "A user friendly and intuitive infrastructure that enables efficient analog mixed-signal verification using assertions based self checking analog designs," CDNLive India 2012
[8] Dhanasekar V, et al, "Analysis of Machine Learning Techniques for Time Domain Waveform Prediction in Analog and Mixed Signal Integrated Circuit Verification.", ISQED 2023.
[9] Lakshmanan Balasubramanian, et al, "Novel Applications of Analog Fault Simulation: ADC, Memory and Package Level Tests," IEEE MDTS, 2022

2. Motivation & Problem Statement (2/2)
Analog Behavioural Model Generation Flow



Limitations of manual model creation

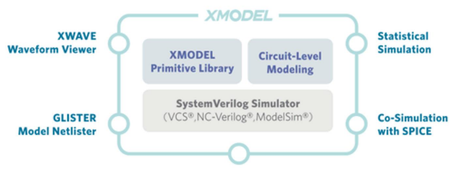
- What to model → Specifications aligned manually project to project
- How much to model? → Fidelity vs. Accuracy
- Conventional scalar real numbered (RN) modelling
  - Can only represent either voltage or current quantity → SV EEnet can help overcome this
  - Some analog functions require both voltage and current modelling

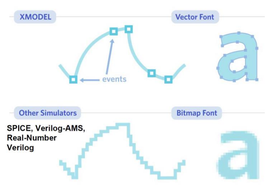
Issues in execution

- Specification based model → Potential missing functionality
- Not true to implementation → Implementation bugs cannot be identified in DV
- Incomplete model validation → Implementation vs. model functionality mismatch

3. Proposed Solution (1/3)

- MODELZEN[10]: An automatic SystemVerilog model generator for analog circuits
- Each unique device characterized and mapped to SystemVerilog based XMODEL[10] primitive





4. Proposed Solution (2/3)

User inputs

Technology configuration file with technology device to XMODEL primitive mapping
SPICE simulation options
Device models and corners
Device mapping
Overriding default MODELZEN options
Importing default configuration

Spectre Netlist

```
M02 (VSS Y A VSS) NCH_3P3V_ESF3 m=1 adasNum=1 osdNum=1 wFinger=0.4 \
    mi=1 cps=0.12 adNum=0 asNum=0 l=0.6 miX=1 asdNum=0 assNum=0
```

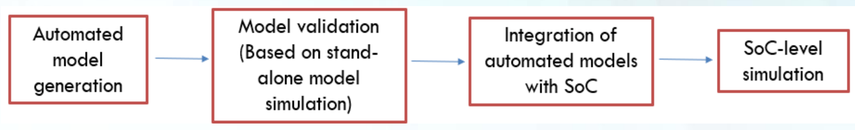
Flow output

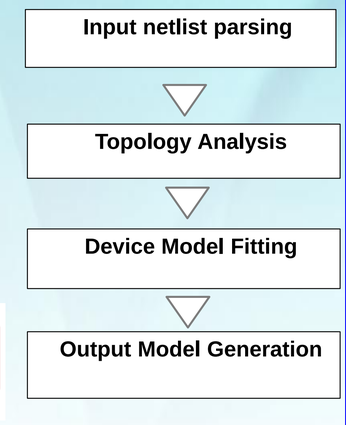
XMODEL primitive mapping

```
nmosfet #(.W(1), .L(0.6), .Kp(4.804e-05), .Vth(1.118), .Cgb('{8.358e-16,1.111e-15,9.44e-16}), .Csb
('{6.649e-16,8.392e-16,1.01e-15}), .Cdb('{6.65e-16,8.392e-16,5.053e-16}), .m(m)) M02 (.d(Y), .g
(A), .s(VSS), .b(`ground));
```

5. Proposed Solution (3/3)

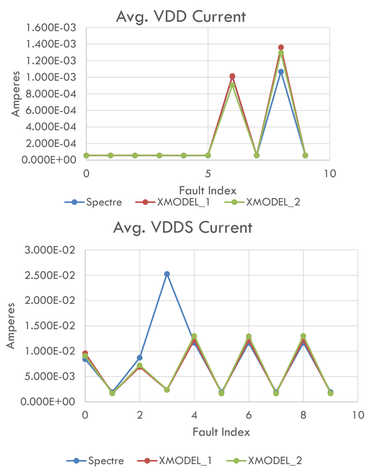
- It preserves the structure of the circuit (i.e., topology)
- MODELZEN is an automatic model generator for analog circuits
- Model is built characterizing the individual devices composing the circuits and connecting the resulting device models according to the topology
- The design flow for model generation in XMODEL

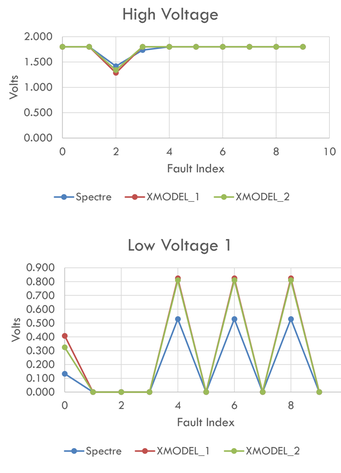


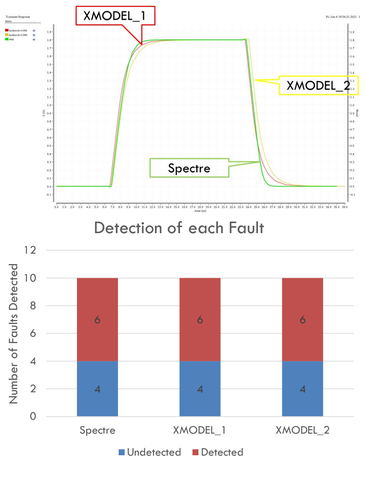


6. Evidence and Results

- Case Study-1: General purpose input and output (GPIO) interface circuit
  - Good match across all specifications between Spectre® netlist and XMODEL based functional simulations
  - Models generated with 2 different accuracy settings
    - XMODEL_1: *level_dc='max_idsat', level_ac=1* for digital circuits
    - XMODEL_2: *level_dc='pwl:3', level_ac=3* for analog circuits
  - As a proof of concept, idea extended to have analog defects modelled using XMODEL
    - 10 out of ~250 defect locations randomly chosen: 100Ω short defects
- Case Study-2: Mixed-signal power management IP models generated for embedded processing, low power, mixed-signal microcontroller
  - On-chip (linear and switching) voltage regulator (VR) supplies, high and low frequency oscillators, bias generator
  - Validated individually and in the context of SoC level DMS/AMS co-sim.







7. Conclusions

- Case-Study-1: GPIO
  - Good match between autogenerated models against Spectre simulation
  - A pilot analog defect/fault simulation capability established
- Case Study-2: MSIPs in LP MS SoC
  - 60 to 99% runtime improvements observed at standalone MSIP level simulations
  - More than 90% runtime improvements against AMS co-sim. at SoC level
  - Significant improvement against conventional model runtimes at SoC level DMS co-sim.
  - Switch circuits (DCDC and oscillators) degrade in performance
  - Better accuracy for model generation to be pursued
  - Several issues found and fixed natively in MODELZEN
  - 2X osc. frequency mismatch observed, manually worked-around by custom frequency divider (tool debug for given technology node

Case Study-2: Manual and Compute Effort Improvements

MSIP	Model Generation Time		Simulation Runtime			
	VAMS Model Creation (days)	XMODEL Generation (hh:mm:ss)	Standalone IP		SoC Level	
			Simulation Time (µs)	Improvement (% of Spectre AMS Runtime)	Improvement (% of Spectre AMS Runtime)	Improvement (% of DMS Runtime w/ Conventional BMODs)
LDO VR1	4	01:40:44	500	**98.61%**	**99.87%**	**69.44%**
LDO VR2	4	01:34:59	1500	**97.67%**	**99.65%**	**19.44%**
DCDC VR	7	01:30:00	5000	**95.61%**	**91.93%**	**-301.11%**
Oscillator-1	4	00:02:05	5000	**63.76%**	**99.80%**	**-28.06%**
Oscillator-2	7	01:40:00	5000	**81.58%**	**96.14%**	**-516.67%**
Bias Generator	2	00:06:21	5000	**99.14%**	**99.65%**	**19.44%**

- Orders of magnitude improvement in the model creation effort → 100x (1-2 weeks to 1-2 hours)
- Orders of magnitude improvement in runtime compared to SPICE/AMS co-sim. with 4 CPU multi-threading → 1000x or more
- No perceivable runtime impact against conventional models → 0.5x on most cases, 1.2-5x for oscillators and switching circuits
- Increased quality with negligible or no overhead → Functionality including current consumption, loading effects, settling behaviour are all automatically captured
- Pioneering analog defect simulation capability in event driven simulator established

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